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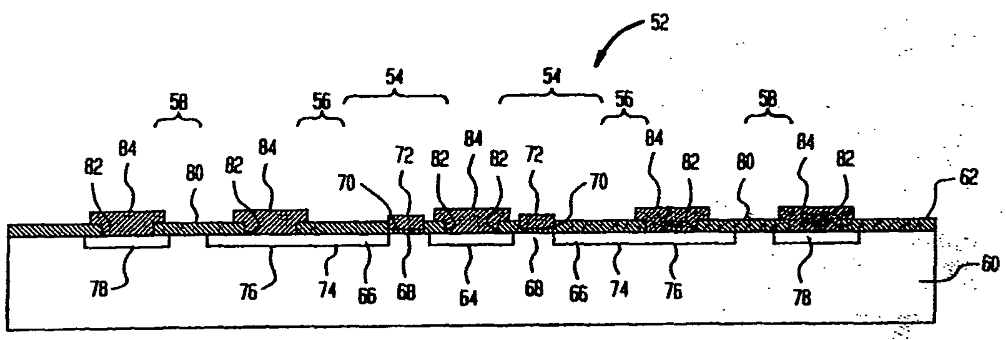

(57) Abstract

An output protection circuit for an integrated circuit includes a plurality of cells (52) formed in a common substrate (60) Each cell (52) includes a pair of MOS transistors (54) having a central source region (64), a pair of drain regions (65) at opposit sides of and spaced from the source region (64), a separate insulated gate (72), and an extension (74) extending from the drai regions (66) away from the source region (64). The extensions (74) are narrower than the source regions (64) to provide a resistor At the end of each of the extensions (74) is a drain contact region (76), and an adjacent highly conductive region (78) of the sam conductivity type as the substrate (60) which forms the contact of one side of a diode (58) formed between each of the drain con tact regions (71) and the substrate (60). The source regions (64), the diode contact regions (78), and the drain contact regions (76 are electrically connected to corresponding common terminals.

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NMOS DEVICE WITH INTEGRAL ESD PROTECTION

Field of the Invention

The present invention relates to an output protection circuit for an integrated circuit, and, more particularly to a NMOS output circuit for protecting the integrated circuit form electrostatic discharge (ESD).

Background of the Invention

Many attempts have been made in the prior art to protect semiconductor devices, including bipolar transistors, field effect devices, and integrated circuit against damage due to voltage and current transients. Some of such protection circuits are described in the United States patents to Stewart, No. 3,967,295, Khajezadeh, No. 4,106,048, Kim, No. 4,342,045, Igarashi, No. 4,656,491, Shirato et al, No. 4,710,791, Leuschner, NO. 4,724,471, Sato, No. 4,739,438, Hatta et al, No. 4,803,527, Clark, No. 4,807,080 and Chen et al, No. 4,825,280.

A particular problem with integrated circuit which include field effect transistors has been their protection from electrostatic discharge (ESD). One type of output circuit which has been used for this purpose is shown in Fig. 1 and is generally indicated as 10. The output circuit 10 includes a plurality of NMOS transistors 12 connected in parallel between an output voltage line 14 and a reference voltage line 16. The gate electrode 18 of each transistor 12 is connected to a common gate terminal 20. The NMOS transistors 12 typically provide a nominal level of protection against electrostatic discharge (ESD) by a parasitic diode 22, shown in phantom in Fig. 2, with its cathode electrode connected to the output voltage line 14 and its anode electrode connected to the reference voltage line 16. The parasitic diode 22 protects against negative voltage transients by shunting the transient energy away from the associated NMOS transistor 12. Each NMOS transistor 12 also provides a parasitic NPN transistor 24, also shown in phantom in Fig. 2. Parasitic transistor 24 has its collector

electrode 26 and its emitter electrode 28 connected to output voltage line 14 and reference voltage line 16 respectively. The base electrode 30 of transistor 24 is connected via a parasitic resistance 32 to the reference voltage line 16. The parasitic NPN transistor 24 protects against positive voltage transients. When the level of a positive transient voltage exceeds the V_{cer} capability of transistor 24, the transistor 24 breaks down and conducts the transient energy from output line 14 to reference line 16, limiting the transient voltage across the associated NMOS transistor 12.

Referring to Fig. 3, there is shown a prior art NMOS output transistor array 34 comprised of a plurality of NMOS transistors 12 connected in parallel. The source regions 36 of the transistors 12 are connected to a common source electrode 38, the drain regions 40 are connected to a common drain electrode 42 and the gate electrodes 44 are connected in common to a primary gate electrode 46. In the array 34, the parasitic diodes 22 are limited in the protection they provide due to their relatively high series resistance. Also, the parasitic transistors 24 are limited in the positive transient protection they provide due to the local concentration of transient current, typically called current focusing.

One technique which has been used to improve the ESD protection provided by the NMOS transistors 12 is to increase the spacing between the gate region and the drain contacts of the transistors by making a long active area region 48, as shown in Fig. 3. This particular technique only offers about a factor of two to three improvement in transient energy handling capability of the array 34, due to the occurrence of current focusing, caused by two or more drain contacts feeding current to a common breakdown region. The current focusing is illustratively shown by the wavy lines in Fig. 3 as occurring at common breakdown regions 49 and 50 which are being fed current from a plurality of drain contacts 40.

In order to prevent the occurrence of current focusing in an NMOS output transistor array , it is necessary to insure that only one contact can deliver current to a given drain/gate

region, and that sufficient resistance is added to the drain region to limit the current flow therethrough. Also, it has been found that the parasitic diode 22 associated with an NMOS transistor 12 is unreliable, and that the diode must be formed deliberately in order to provide protection against negative voltage transients. Therefore, it is desirable to have a NMOS transistor array protection circuit which eliminates or reduces current focusing and provides a protection diode therein.

Summary of the Invention

The invention provides an improved NMOS output transistor having improved current limiting and substantially reduced current focusing and includes a deliberately formed diode for improved protection from negative transients. The invention is also a structure which includes a plurality of individual NMOS transistors connected in parallel and formed on a common substrate with means for both limiting the current flow in the drain/gate region of an NMOS transistor and providing electrical isolation between the various drain contacts, thereby substantially insuring that only one drain contact can conduct current to an associated gate region, thereby preventing current concentration from adjacent drain contacts.

Brief Description of the Drawings

Fig. 1 is a partial schematic circuit diagram of a prior art integrated circuit output transistor configuration.

Fig. 2 is a schematic circuit diagram showing parasitic ESD and transient voltage protective elements provided by each paralleled connected transistor of Fig. 1.

Fig. 3 is a top plan view of an integrated circuit including the structural layout for a typical prior art NMOS output transistor array.

Fig. 4 is a cross section of one form of an NMOS output transistor structure of the present invention.

Fig. 5 is a top plan view of the transistor shown in Fig. 4.

Fig. 6 is a schematic circuit diagram of the transistor shown in Figs. 4 and 5.

Fig. 7 is a top plan view of the structural layout of a NMOS output transistor array of the present invention.

Detailed Description of Preferred Embodiment

Referring to Figs. 4 and 5, there is shown a form of a cell 52 of the protection circuit of the present invention. The cell 52 comprises two NMOS transistors 54, two resistors 56 and two diodes 58. The cell 52 is formed in a substrate 60 of a semiconductor material, such as single crystalline silicon, of lightly doped P-type conductivity (P-) having a doping concentration of about 10^{13} cm^{-3}. It should be noted that instead of forming the cell 52 in a P- substrate 60, it can be formed in a P- well in the substrate 60. In the substrate 60 at its surface 62 is a centrally located highly conductive N-type conductivity (N+) source region 64 having a doping concentration of about 10^{18} cm^{-3}. In the substrate 60 at the surface 62 and at opposite sides of the source region 64 are highly conductive N-type conductivity (N+) drain regions 66. The drain regions 66 are spaced from the source region 64 to form channel regions 68 in the substrate 60 between the source region 64 and each of the drain regions 66. A thin layer 70 of an insulating material, such as silicon dioxide, is on the substrate surface 62 over each of the channel regions 68, and a conductive gate 72, typically of doped polycrystalline silicon, is on each of the channel insulating layers 70. Thus, the source region 64, drain region 66 and gates 72 form the transistors 54.

Each of the drain regions 66 has an extension 74 extending therefrom away from the source region 64. The extension 74 is narrower than the drain region 66 and forms a resistor 56. At the end of each of the extensions 74 away from the drain region 66 is a contact pad region 76 which is wider than the extension 74 but narrower than the drain region 66. In the substrate 60 adjacent to but spaced from each of the contact pad regions 76 is a region 78 of highly conductive P-

type conductivity (P+). The region 78 serves as the contact pad for the anode of a diode 58 formed between the N+ type contact pad region 76 and the P- substrate 60. A layer 80 of an insulating material, such as silicon oxide or a glass, is over the substrate surface 62 and covers the source region 64, the drain regions 66, resistors extensions 74, contact pad regions 76 and P+ regions 78. The insulating layer 80 has openings 82 therethrough over the source region 64, each of the contact pad regions 76 and each of the P+ regions 78. Separate metal contacts 84 extend through the openings 80 to make electrical contact with each of the regions at the bottom of the openings.

Referring to Fig. 6, there is shown a simplified schematic circuit diagram of one-half of a cell 52. The drain 66 of a NMOS transistor 54 is connected through a resistor 56, formed by the extension 74, to an output voltage line 86, and the source 64 is connected to a reference voltage line 88. The diode 58 formed between the bonding pad 76 and the substrate 60 is connected between the output voltage line 86 and the reference voltage line 88 in parallel with the transistor 54. In the cell 52 there is formed a parasitic NPN transistor 92 which has an emitter 94 provided by the source region 64 of the transistor 56, a collector 96 provided by the drain region 66 of the transistor 56 and a base 98 provided by the substrate 60. The substrate 60 also provides a base resistor 100.

Fig. 7 shows an NMOS output transistor array 102 comprising a plurality of the cells 52 connected in parallel with one another. The cells 52 are arranged in a plurality of columns with the source regions 64 of the transistors 54 in each column being connected to a source contact pad 104 by a common connecting strip 106. The drain contact pads 76 are connected to a common drain contact pad 108 by a common connecting strip 110. The gates 72 are connected to a gate bus 112 by a connecting strip 114. The anode pad regions 78 are electrically connected to the source contact pad 104 by connecting strips 116.

In the operation of the array 102 having the cells 52 of the present invention, only one drain contact pad region 76 can

feed current to an associated channel region 68. Under a positive transient voltage, the parasitic NPN transistor 92 of a given cell 52 goes into a "snap-back" mode of operation at a given current level, and the main power dissipation occurs at the associated gate/drain area. If one such gate/drain area tends to break down at a lower voltage than other gate/drain areas, current concentration is by the drain contact pads 76 being spaced from the drain region 66 and by the resistor extension 74 therebetween. Also, since the resistor extension 74 are narrower than the drain regions 66, there is provided relatively large spaces 118, see Fig. 7, between each drain pad region 76 and the drain region 66 of adjacent transistors 56. These spaces 118 electrically isolate the drain pad regions 76 from the drain regions 66 of adjacent transistors 56 so as to prevent current focusing. The insulating layer 80 which extends over the substrate surface 64 including the spaces 118 provides additional insulation in the spaces 118. Finally, in the array 102, each of the diodes 58 is specifically formed so that it is more reliable than the previously provided parasitic diode to insure proper operation of the protection circuit. Thus, there is provided by the present invention an NMOS protection circuit which includes an array of NMOS transistors which provides the desired protection against electrostatic discharge and minimizes current focusing.

Modification of the various embodiments of the invention may occur to one skilled in the art. For example, while the exemplary embodiment has been described in terms of particular conductivity types, converse conductivity types may be used so long as the relative conductivity types remain the same. Such and like modifications are intended to be within the spirit and scope of the invention, and the appended claims.

What is claimed is:

1. A protection circuit comprising a plurality of integrated circuit cells connected in parallel in an array, wherein each of said cells comprises:

a common substrate of a first conductivity type having a surface;

a first region of second conductivity type in the substrate at said surface forming a source of a MOS transistor;

a second region of second conductivity type in the substrate at said surface and spaced from the first region forming a drain of the transistor with the portion of the substrate between the first and second regions forming the channel of the transistor;

gate means overlying and insulated from the substrate surface between the first and second regions and over the channel;

an extension of said second region extending along the substrate surface from the second region away from the channel, said extension being narrower than the second region; and

a drain contact region of the second conductivity type of relatively high conductivity in said substrate at said surface and at the end of the extension.

2. The protection circuit of claim 1 including a third region of the first conductivity type in the substrate at said surface, said third region being adjacent to but spaced from the drain contact region forming the contact to one side of a diode formed between the substrate and the drain contact.

3. The protection circuit of claim 2 including a layer of an insulating material over the surface of the substrate, and the gate is on a portion of the insulating layer over the channel.

4. The protection circuit of claim 3 separate conductor means extending through openings in the insulating layer and contacting the first, second and third regions respectively.

5. The protection circuit of claim 2 in which the drain contact is narrower than the second region but wider than the extension.

6. The protection circuit of claim 1 including a fourth region of the second conductivity type in the substrate at said surface on the side of the first region opposite from the second region, said fourth region being spaced from the first region to form a second drain region with a second channel between the first and fourth regions, and a second gate over and insulated from the surface of the substrate along said second channel.

7. The protection circuit of claim 6 including an extension of the fourth region extending along said substrate surface from the fourth region away from the second channel, said extension being narrower than the fourth region.

8. The protection circuit of claim 7 including a drain contact region of the second conductivity type and of relatively high conductivity in the substrate at said surface at the end of the extension from the fourth region.

9. The protection circuit of claim 8 including a fifth region of the one conductivity type in the substrate at said surface, said fifth region being adjacent to but spaced from the drain contact region for the fourth region and forming the contact to one side of a diode formed between the substrate and the drain contact region for the fourth region.

10. The protection circuit of claim 9 in which the drain contact region for the fourth region is wider than the extension from the fourth region but narrower than the fourth region.

11. The protection circuit of claim 9 including a layer of an insulating material over the substrate surface, and the gates are on the insulating material over their respective channels.

12. The protection circuit of claim 11 including a separate conductor extending through the insulation layer and electrically contacting the first, second, third, fourth and fifth regions respectively.

13. The protection circuit of claim 12 in which the cells are arranged in columns, and in each column means electrically connecting together the conductors for each of the first, second, third, fourth and fifth regions respectively.

14. The protection circuit of claim 13 in which the means electrically connecting together the first regions of each of the columns are electrically connected to a common source terminal pad, the means electrically connecting the second and fourth regions are electrically connected to a common drain terminal pad, the means electrically connecting the fifth regions are electrically connected to the source terminal pad, and the gates are electrically connected to a common gate bus.

15. A transient protection circuit comprising at least on cell, said cell comprising:

a substrate of a first conductivity type having a surface;

a first region of a second conductivity type in the substrate at said surface;

a second region of a second conductivity type in the substrate at said surface and spaced from said first region;

a thin layer of an insulating material over said substrate surface between said first and second regions;

a conductive gate on said insulating material layer and over the space between the first and second regions;

an extension of said second region extending along said substrate surface from the second region away from the first region, said extension being narrower than the second region;

a contact region of the second conductivity type in said substrate at said surface at the end of the extension of the second region; and

a third region of the one conductivity type in the substrate at said surface adjacent to but spaced from the contact region.

16. The protection circuit of claim 15 further comprising:

a fourth region of the second conductivity type in the substrate at said surface adjacent to but spaced from the first region and on the side of the first region opposite the second region;

a thin layer of an insulating material on the substrate surface between the first and fourth regions;

a conductive gate on the insulating layer and between the first and fourth regions;

an extension of said fourth region extending along said substrate surface from the fourth region away from the first region, said extension being narrower than the fourth region;

a contact region of the second conductivity type in the substrate at said surface at the end of the extension of the fourth region; and

a fifth region of the one conductivity type in the substrate at said surface adjacent to but spaced from the contact region for the fourth region.

17. The protection circuit of claim 16 including a plurality of said cells in said substrate arranged in columns, means connecting together all of the first regions of the cells in each column, means connecting together the contact regions for the second regions in each column, means connecting together the third regions in each column, means connecting together the contact regions for the fourth regions in each column, means connecting together the fifth regions in each column and means connecting together the gates in each column.

18. The protection circuit of claim 17 in which the means connecting together the first regions are electrically connected to a first terminal pad, the means connecting together the contact regions for the second and fourth regions are connected to a second terminal pad, the means connecting together the third and fifth regions are connected to the first terminal pad, and the means connecting together the gates are connected to a common bus line.

FIG. 1
(PRIOR ART)

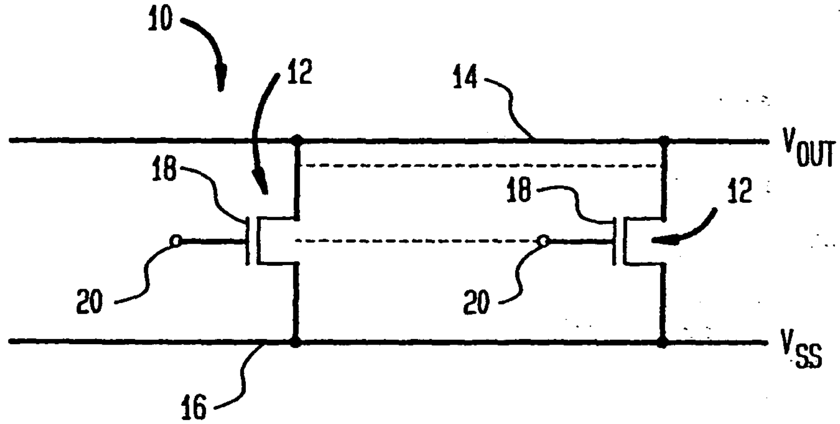


FIG. 2
(PRIOR ART)

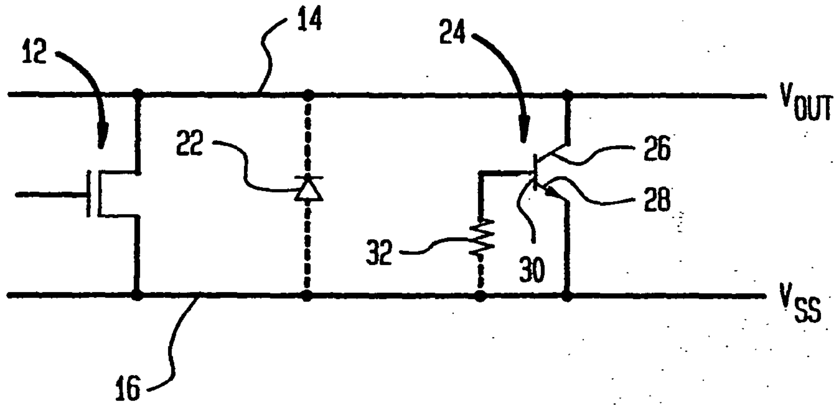


FIG. 6

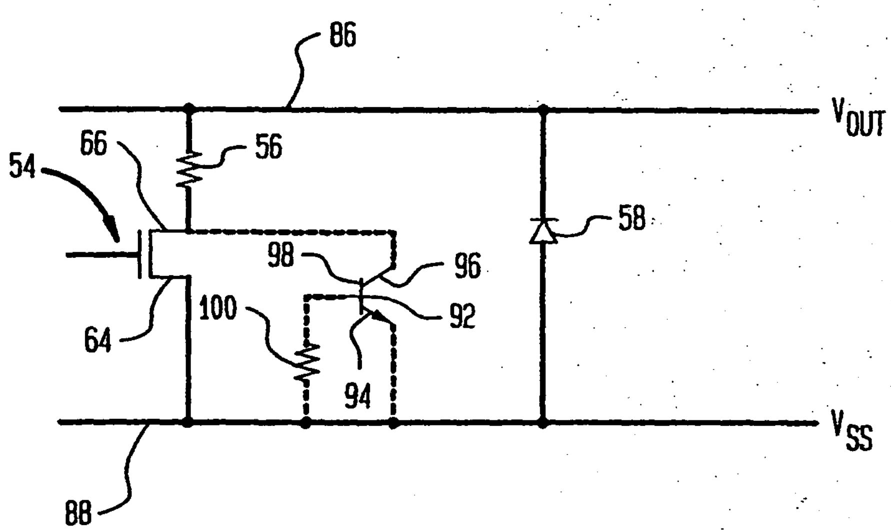
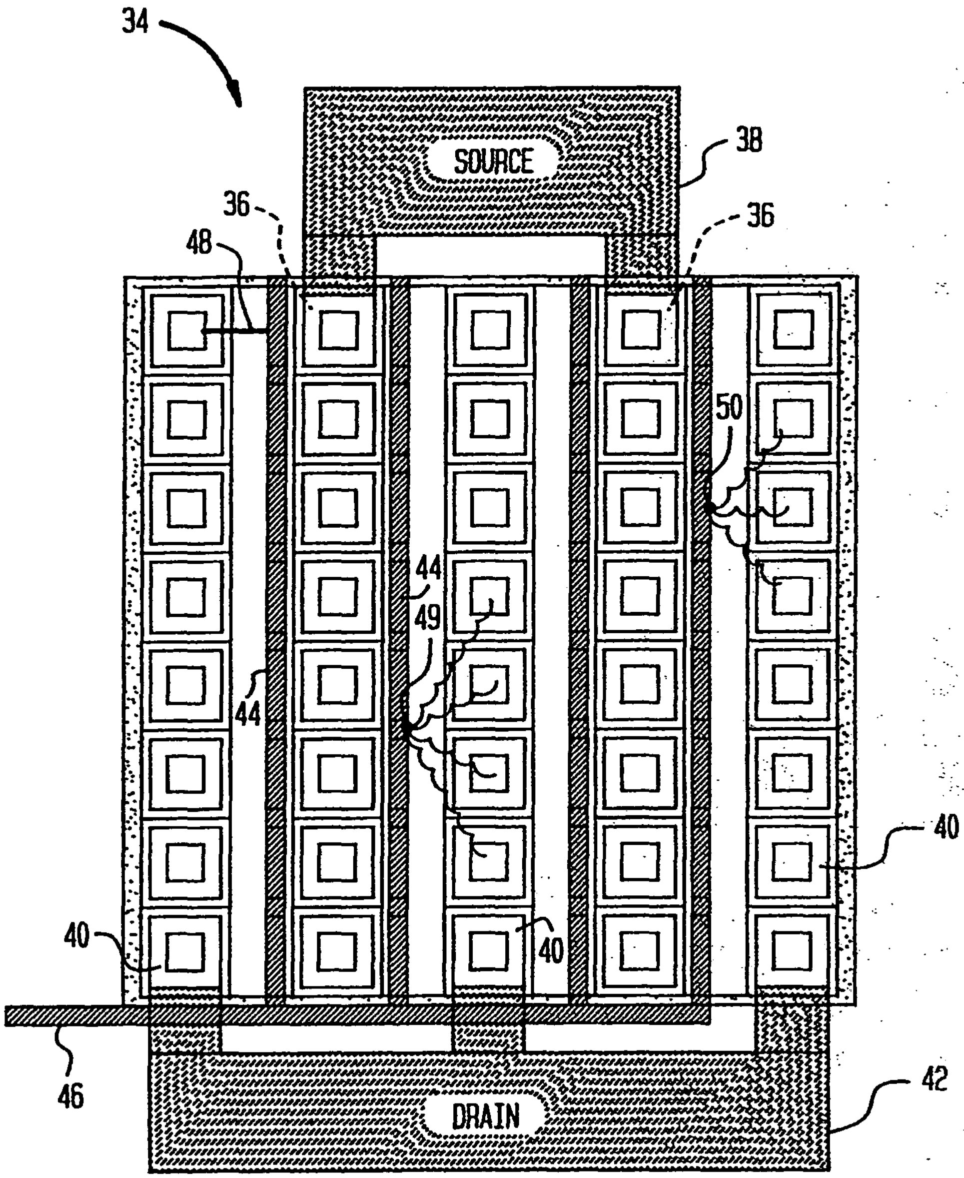


FIG. 3
(PRIOR ART)



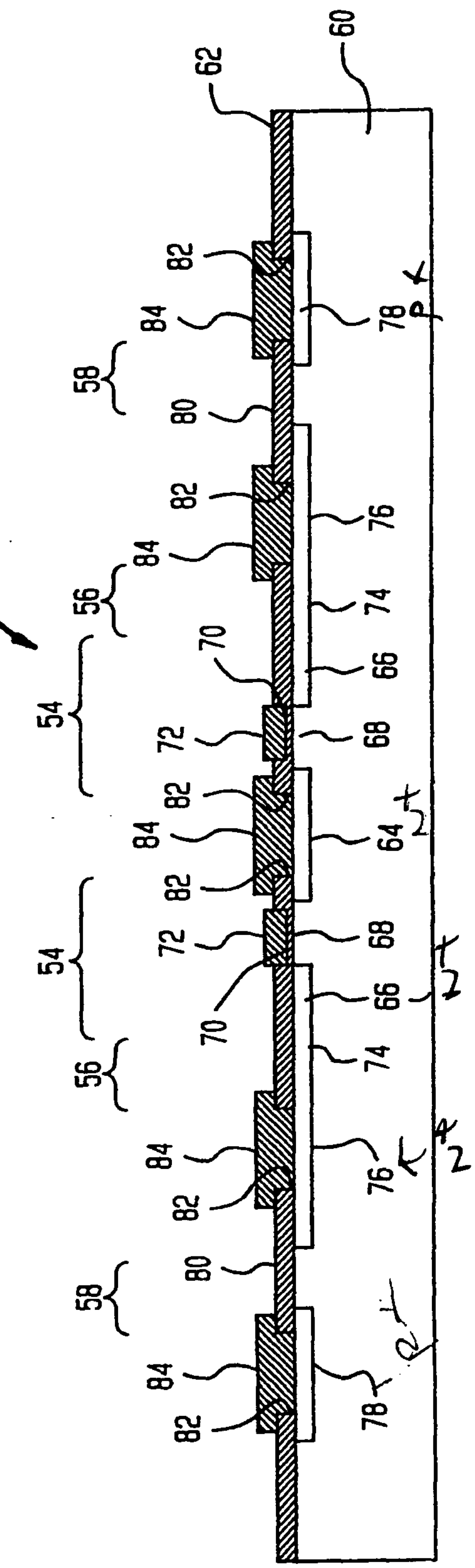

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FIG. 4

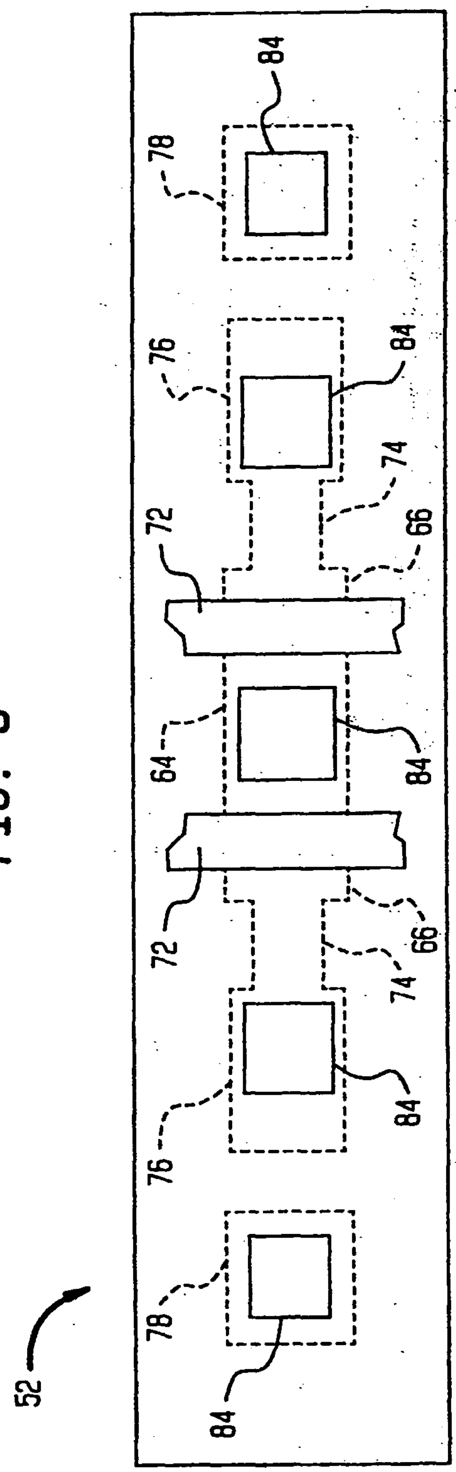
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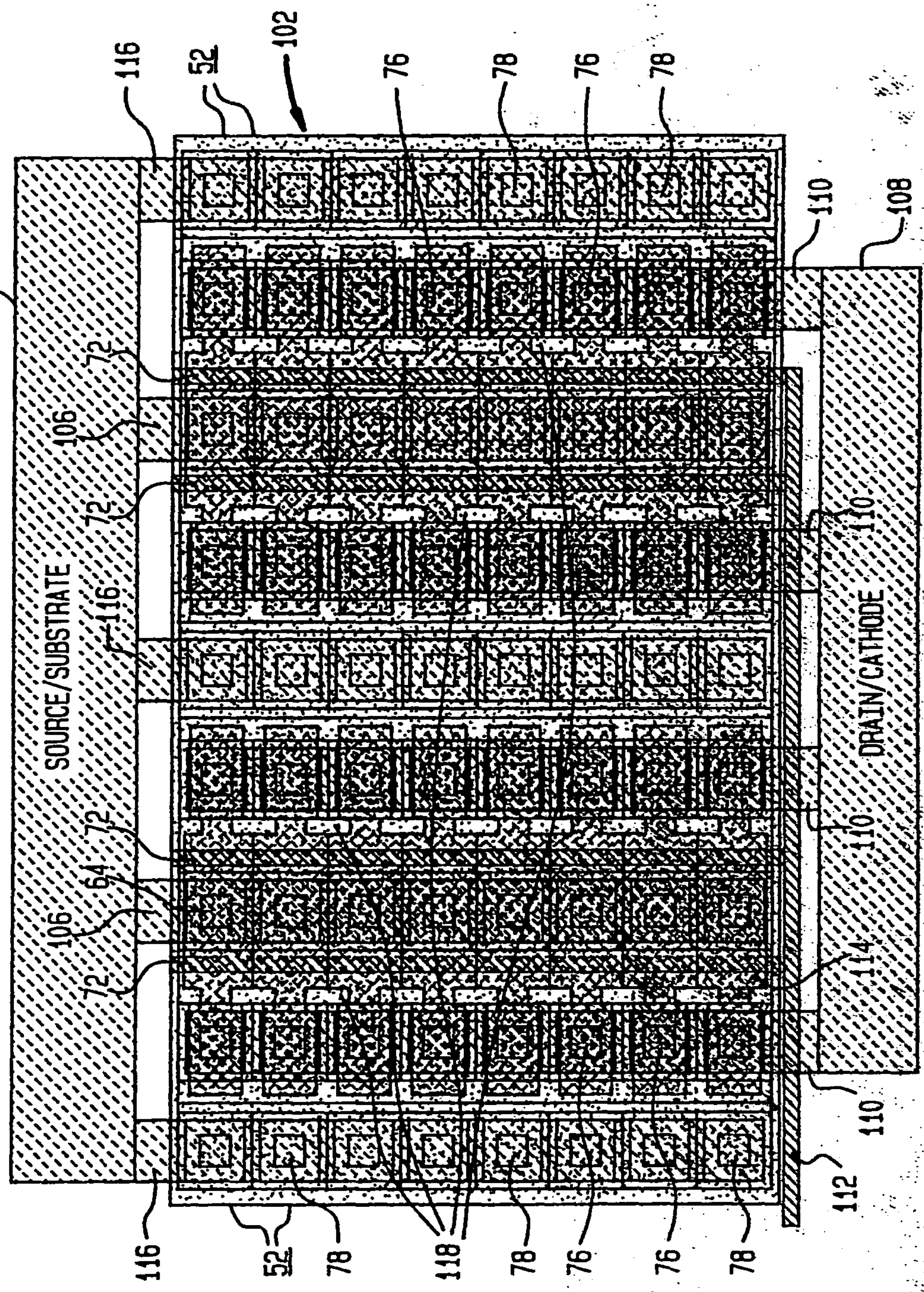
FIG. 5

FIG. 7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INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/05175

I. CLASSIFICATI N OF SUBJECT MATTER (if several classification symbols apply, indicate all)

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IPC 5 H01L 27/088 11 H01L 29/784

U.S. 357/23.8 11 357/23.13

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Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
X Y	US, A, 4,845,536 Heinecke et. al. 04 July 1989. (See the whole document).	1,6-8 2-5,9-18
&,X Y	JP, A 60-158671 Tekisasu Insutsurumentsu 20 August 1985. (See the whole document).	1, 6-8 2-5, 9-18
P,Y	JP, A 2-1965 Samsung Electronics. 08 January 1990.	2-5, 9-18
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